16-Bit, 6MSPS PulSAR Differential ADC

Preliminary Technical Data

AD7625

FEATURES

Throughput: 6 MSPS
SAR architecture
16-bit resolution with no missing codes
SNR: 92 dB Typ, 90dB Min @ 1MHz
INL: ±1 LSB Typ, ±2 LSB Max
DNL: ±0.3 LSB Typ, ±1 LSB Max
Differential input range: ± 4.096V
No latency/no pipeline delay (SAR architecture)
Serial LVDS interface:
- **Self-clocked mode**
- **Echoed-clock mode**

Reference:
- **Internal 4.096 V**
- **External (1.2V) buffered to 4.096 V**
- **External 4.096 V**

Power dissipation 150 mW
32-Lead LFCSP package (5 mm x 5 mm)

APPLICATIONS

High dynamic range telecommunications Receivers
Digital imaging systems
High-speed data acquisition
Spectrum analysis
Test equipment

Table 1. Fast PulSAR ADC Selection

Input Type	Res (Bits)	≥1 MSPS to < 2MSPS	≥ 2 MSPS to ≤ 3 MSPS	6 MSPS	10 MSPS
Differential (ground sense)	16	AD7653 AD7667 AD7980 AD7983	AD7985		
True Bipolar	16	AD7671			
Differential (anti-phase)	16	AD7677 AD7623	AD7621 AD7622	AD7625	AD7626
Differential (anti-phase)	18	AD7643 AD7982 AD7984	AD7641 AD7986		

FUNCTIONAL BLOCK DIAGRAM

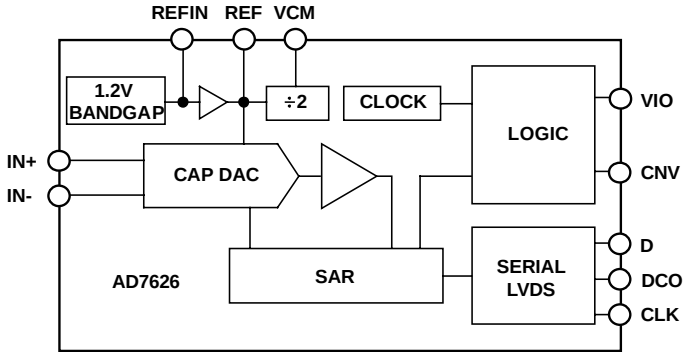

Figure 1.

GENERAL DESCRIPTION

The AD7625 is a 16-bit, 6MSPS, charge redistribution successive approximation register (SAR) architecture, analog-to-digital converter (ADC). SAR architecture allows unmatched performance both in noise – 92dB SNR - and in linearity – 1LSB. The AD7625 contains a high speed 16-bit sampling ADC, an internal conversion clock, and an internal buffered reference. On the CNV edge, it samples the voltage difference between IN+ and IN− pins. The voltages on these pins swing in opposite phase between 0 V and REF. The 4.096V reference voltage, REF, can be generated internally or applied externally.

All converted results are available on a single LVDS self-clocked or echoed-clock serial interface reducing external hardware connections.

The AD7625 is housed in a 32-lead LFCSP (5mm by 5mm) with operation specified from −40°C to +85°C.

Rev. PrB

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SPECIFICATIONS

VDD1 = 5 V; VDD2 = 2.5 V; VIO = 2.5 V; V_{REF} = 4.096 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
RESOLUTION		16			Bits
ANALOG INPUT					
Voltage Range	$V_{IN+} - V_{IN-}$	$-V_{REF}$		$+V_{REF}$	V
Operating Input Voltage	V_{IN+}, V_{IN-} to AGND	−0.1		$+V_{REF}$ + 0.1	V
Common Mode Input Range		$V_{REF}/2 - 0.1$	$V_{REF}/2$	$V_{REF}/2 + 0.1$	V
Analog Input CMRR	f_{IN} = 1 MHz		60		dB
Input Current	6 MSPS throughput		350		µA
THROUGHPUT SPEED					
Complete Cycle				166	ns
Throughput Rate		0.001		6	MSPS
DC ACCURACY					
Integral Linearity Error		-2	±1	+2	LSB
No Missing Codes		16			Bits
Differential Linearity Error		-1	±0.3	+1	LSB
Transition Noise			0.6		LSB
Zero Error, T_{MIN} to T_{MAX}			±100		µV
Zero Error Drift			1		ppm/°C
Gain Error, T_{MIN} to T_{MAX}			50		ppm of FS
Gain Error Drift			1		ppm/°C
Power Supply Sensitivity	VDD1 = 5 V ± 5%		TBD		LSB
	VDD2 = 2.5 V ± 5%		TBD		LSB
AC ACCURACY					
Dynamic Range		90	92		dB
Signal-to-Noise	f_{IN} = 250 kHz	90	92		dB
Spurious-Free Dynamic Range	f_{IN} = 250 kHz		110		dB
	f_{IN} = TBD		90		dB
Total Harmonic Distortion	f_{IN} = 250 kHz		-110		dB
	f_{IN} = TBD		-90		dB
Signal-to-(Noise + Distortion)	f_{IN} = 250 kHz		92		dB
−3 dB Input Bandwidth			100		MHz
Aperture Delay					ns
Aperture jitter			5		ps rms
Transient Response	Full-Scale Step		50		ns
INTERNAL REFERENCE					
Output Voltage	REFIN @ 25°C		1.2		V
Temperature Drift	−40°C to +85°C		±7		ppm/°C
REFERENCE BUFFER					
REFIN Input Voltage Range			1.2		V
REF Output Voltage range			4.096		V
EXTERNAL REFERENCE					
Voltage Range	REF		4.096		V
VCM	@ 25°C				
Output Voltage			$V_{REF}/2$		$V_{REF}/2$
Output Impedance		4	5	6	kΩ

Parameter	Conditions	Min	Typ	Max	Unit
LVDS I/O, (ANSI-644)					
Data Format			Serial LVDS Two's complement		
V_{OD}	Differential Output Voltage, R_L=100 Ω	247	350	454	mV
V_{OCM}	Common mode Output Voltage, R_L=100Ω	1125	1250	1375	mV
V_{ID}	Differential Input Voltage	100		650	mV
V_{ICM}	Common mode Input Voltage	800		1575	mV
POWER SUPPLIES					
Specified Performance					
VDD1		4.75V	5	5.25V	V
VDD2		2.37	2.5	2.63	V
VIO		2.3	2.5	2.7	V
Operating Currents					
VDD1			10		mA
VDD2			25		mA
VIO	Self-clocked mode		14		mA
VIO	Echoed-clock mode		18		mA
Power Dissipation[1]					
With Internal Reference	6 MSPS throughput		140		mW
Without Internal Reference	6 MSPS throughput		120		mW
Energy per conversion	6 MSPS throughput		10		nJ/sample
TEMPERATURE RANGE					
Specified Performance	T_{MIN} to T_{MAX}	−40		+85	°C

[1] Power dissipation is for the AD7626 only. In self-clocked interface, 9mW is dissipated in the 100 ohm terminator. In echoed-clock interface, 18mW is dissipated in (2) 100 ohm terminators.

TIMING SPECIFICATIONS

VDD1 = 5 V; VDD2 = 2.5 V; VIO = 2.3V to 2.7 V; V_{REF} = 4.096 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit
Time between conversion	t_{CYC}	100			ns
Acquisition time	t_{ACQ}	40		10000	ns
CNV high time	t_{CNVH}	10		40	ns
CNV to D (MSB) delay	t_{MSB}			166	ns
CNV to last CLK (LSB) delay	t_{CLKL}			120	ns
CLK period	t_{CLK}	TBD	4		ns
CLK frequency	f_{CLK}		250	400	MHz
CLK to DCO delay (echoed-clock mode)	t_{DCO}	0	4	7	ns
DCO to D delay (echoed-clock mode)	t_D	-1	0	1	ns
CLK to D delay	t_{CLKD}	0	4	7	ns

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	With Respect to	Rating
Analog Inputs/Outputs		
CAP1, REFIN	GND	-0.3V to 2.7V
IN+, IN-, REF, REF/2, CAP2	GND	-0.3V to 6V
Digital Inputs/Outputs	GND	-0.3V to 2.7V
Supply Voltage		
VDD1	GND	-0.3V to 6V
VDD2, VIO	GND	-0.3V to 2.7V

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

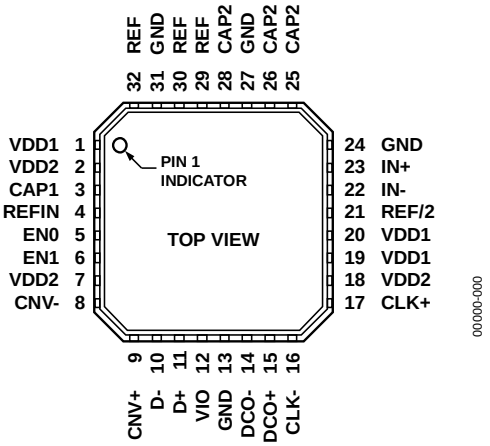


Figure 2.

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1	VDD1	P	Analog 5V Supply. Decouple with 10uF and 100nF capacitors.
2	VDD2	P	Analog 2.5V Supply. The system 2.5V supply should supply this pin first, decoupled with 10uF and 100nF capacitors, then starred off to other VDD2 pins.
3	CAP1	AO	Connect to a 10nF capacitor.
4	REFIN	AI/O	Pre-Buffer Reference Voltage. When using the internal reference, this pin outputs the band-gap voltage and is nominally at 1.2V. It can be overdriven with an external reference voltage like the ADR280. In either mode, a 10uF capacitor is required. If using an external 4.096V reference (connected to REF), this pin is a no connect and does not require any capacitor.
5, 6	EN0, EN1	DI	Enable Pins.
7	VDD2	P	Digital 2.5V supply.
8, 9	CNV-, CNV+	DI	Convert Input. This input has multiple functions. On its rising edge, it samples the analog inputs and initiates a conversion cycle. CNV+ works as a CMOS input when CNV- is grounded otherwise CNV+, CNV- are LVDS inputs.
10, 11	D-, D+	D0	LVDS Data Outputs. The conversion data is output serially on these pins.
12	VIO	P	Input/Output Interface Supply. Nominally 2.5V.
13	GND	P	Ground.
14, 15	DCO-, DCO+	DI/O	LVDS Buffered Clock Outputs. When DCO+ is grounded, the self-clock interface mode is selected. In this mode, the 16 bit results on D is preceded by a three bit header (010) to allow synchronization of the data by the digital host with simple logic. When DCO+ is not grounded, the echoed clock interface mode is selected. In this mode, DCO± is a copy of CLK±. The data bits are output on the falling edge of DCO+ and can be latched in the digital host on the next rising edge of DCO+.
16, 17	CLK-, CLK+	DI	LVDS Clock Inputs. This clock shifts out the conversion results on the negative edge of CLK+.

EN1	EN0	Operation
0	0	Power down all; ADC, internal reference and reference buffer.
0	1	Enable internal buffer, disable internal reference. An external 1.2V reference connected to REFIN pin is required.
1	0	Disable internal reference and buffer. An external reference connected to the REF pin is required.
1	1	Enable all; ADC, internal reference and reference buffer.

Pin No.	Mnemonic	Type[1]	Description
18	VDD2	P	Analog 2.5V Supply.
19, 20	VDD1	P	Analog 5V supply. Isolate from Pin 1 with a ferrite bead.
21	VCM	AO	Common Mode Output. When using any reference scheme, this pin produces ½ of the voltage present on the REF pin which can be useful for driving the common mode of the input amplifiers.
22	IN-	AI	Differential Negative Analog Input. Referenced to and must be driven 180° out of phase with IN+.
23	IN+	AI	Differential Positive Analog Input. Referenced to and must be driven 180° out of phase with IN-.
24	GND	P	Ground.
25, 26, 28	CAP2	AO	Connect all three pins to a single 10uF X5R capacitor with the shortest distance. The other side of the capacitor must be placed close to pin 27 (GND).
27	GND	P	Ground. Return path for 10uF capacitor connected to pins 25, 26, and 28.
29, 30, 32	REF	AI/O	Buffered Reference Voltage. When using the internal reference or 1.2V external reference (REFIN input), the 4.096V system reference is produced at this pin. When using an external reference, like the ADR434 or ADR444, the internal reference buffer must be disabled. In either case, connect all three pins to a single 10uF X5R capacitor with the shortest distance. The other side of the capacitor must be placed close to pin 31 (GND)
31	GND	P	Ground. Return path for 10uF capacitor connected to pins 29, 30, and 32.

[1] AI = analog input; AI/O = bidirectional analog; AO = analog output; DI = digital input; DI/O = bidirectional digital; DO = digital output; P = power.

TERMINOLOGY

Least Significant Bit (LSB)

The least significant bit, or LSB, is the smallest increment that can be represented by a converter. For a fully differential input ADC with N bits of resolution, the LSB expressed in volts is

$$LSB\ (V) = \frac{V_{INp\text{-}p}}{2^N}$$

Integral Nonlinearity Error (INL)

Linearity error refers to the deviation of each individual code from a line drawn from negative full scale through positive full-scale. The point used as negative full scale occurs a ½ LSB before the first code transition. Positive full scale is defined as a level 1½ LSBs beyond the last code transition. The deviation is measured from the middle of each code to the true straight line.

Differential Nonlinearity Error (DNL)

In an ideal ADC, code transitions are 1 LSB apart. Differential nonlinearity is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

Zero Error

The difference between the ideal midscale input voltage (0 V) and the actual voltage producing the midscale output code.

Gain Error

The first transition (from 100 ... 00 to 100 ... 01) should occur at a level ½ LSB above nominal negative full scale (−4.095938 V for the ±4.096V V range). The last transition (from 011 … 10 to 011 … 11) should occur for an analog voltage 1½ LSB below the nominal full scale (+4.095813 V for the ±4.096V range). The gain error is the deviation of the difference between the actual level of the last transition and the actual level of the first transition from the difference between the ideal levels.

Dynamic Range

Dynamic range is the ratio of the rms value of the full scale to the rms noise measured for an input typically at −60 dB. The value for dynamic range is expressed in decibels.

Signal-to-Noise Ratio (SNR)

SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

Total Harmonic Distortion (THD)

THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in decibels.

Signal-to-(Noise + Distortion) Ratio (SINAD)

SINAD is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in decibels.

Spurious-Free Dynamic Range (SFDR)

The difference, in decibels (dB), between the rms amplitude of the input signal and the peak spurious signal.

Effective Number of Bits (ENOB)

ENOB is a measurement of the resolution with a sine wave input. It is related to SINAD and is expressed in bits by

$$ENOB = [(SINAD_{dB} - 1.76)/6.02]$$

Aperture Delay

Aperture delay is a measure of the acquisition performance measured from the falling edge of the $\overline{\text{CNVST}}$ input to when the input signal is held for a conversion.

Transient Response

The time required for the AD7634 to achieve its rated accuracy after a full-scale step function is applied to its input.

Reference Voltage Temperature Coefficient

Reference voltage temperature coefficient is derived from the typical shift of output voltage at 25°C on a sample of parts at the maximum and minimum reference output voltage (V_{REF}) measured at T_{MIN}, T(25°C), and T_{MAX}. It is expressed in ppm/°C as

$$TCV_{REF}(\text{ppm/°C}) = \frac{V_{REF}\ (Max) - V_{REF}\ (Min)}{V_{REF}\ (25°\text{C}) \times (T_{MAX} - T_{MIN})} \times 10^6$$

where:
$V_{REF}\ (Max)$ = maximum V_{REF} at T_{MIN}, T(25°C), or T_{MAX}.
$V_{REF}\ (Min)$ = minimum V_{REF} at T_{MIN}, T(25°C), or T_{MAX}.
$V_{REF}\ (25°C)$ = V_{REF} at 25°C.
T_{MAX} = +85°C.
T_{MIN} = −40°C.

THEORY OF OPERATION

Echoed-Clock Interface Mode

The AD7626 digital operation in "echoed-clock interface mode" is shown in Figure 3. This interface mode, requiring just a shift register on the digital host, can be used with many digital hosts (FPGA, shift register, microprocessor, etc.). It requires 3 LVDS pairs (D±, CLK±, and DCO±) between each AD7626 and the digital host.

The clock DCO is a buffered copy of CLK and synchronous to the data, D, which is updated on DCO+ falling edge (t_D). By keeping good propagation delay matching between D and DCO through the board and the digital host, DCO can be can be used to latch D with good timing margin for the shift register.

Conversions are initiated by a CNV pulse. The CNV must be returned low ≤ t_{CNVH}(max) for valid operation. Once a conversion has begun, it continues until completion. Additional CNV pulses are ignored during the conversion phase. After the time t_{MSB} elapses, the host should begin to burst the CLK. Note that t_{MSB} is the maximum time for the MSB of the new conversion result and should be used as the gating device for CLK. The echoed clock, DCO, and data, D, will be driven in phase with D being updated on the DCO+ falling edge and the host should use the DCO+ rising edge to capture D. The only requirement is that the 16 CLK pulses finish before the time t_{CLKL} elapses of the next conversion phase or the data will be lost. From the time t_{CLKL} to t_{MSB}, D and DCO will be driven to 0's.

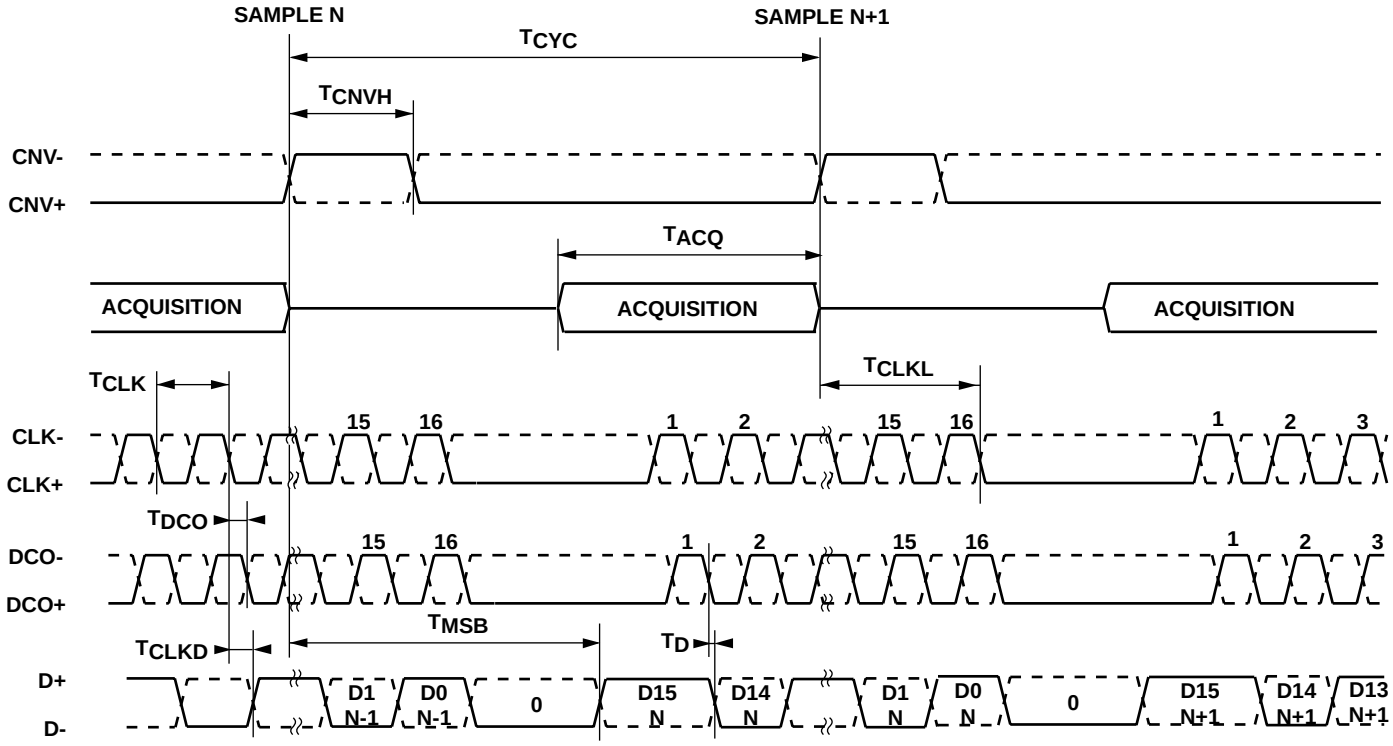


Figure 3. Echoed-Clock Interface Mode Timing Diagram

Self Clocked Mode

The AD7626 digital operation in "self-clocked interface mode" is shown in Figure 4. This interface mode reduces the number of wires between ADCs and the digital host to 2 LVDS pairs per AD7626, CLK± and D± or a single pair if sharing a common CLK using multiple AD7626's. This considerably eases the design of a system using multiple AD7626's since the interface can tolerate several CLK cycles of propagation delay mismatch between the different AD7626 devices and the digital host.

The "self-clocked interface mode" consists of preceding each ADC word results by a header of 2 bits on the data, D This header is used to synchronize D of each conversion in the digital host. Synchronization is accomplished by one simple state machine per AD7626 device. The state machine is running, for instance, at the same speed as CLK with 3 phases. The state machine measures when the first "one" of the header occurs. This provides the value of the actual propagation delay delta between the state machine clock and D including any board propagation time allowing to use the best clock signal to latch the following bits of the conversion result.

Conversions are initiated by a CNV pulse. The CNV must be returned low ≤ t_{CNVH}(max) for valid operation. Once a conversion has begun, it continues until completion. Additional CNV pulses are ignored during the conversion phase. After the time t_{MSB} elapses, the host should begin to burst the CLK. Note that t_{MSB} is the maximum time for the first bit of the header and should be used as the gating device for CLK. CLK is also used internally on the host to begin the internal synchronization state machine. The next header bit and conversion results are output on subsequent falling edges of CLK. The only requirement is that the 18 CLK pulses finish before the time t_{CLKL} elapses of the next conversion phase or the data will be lost.

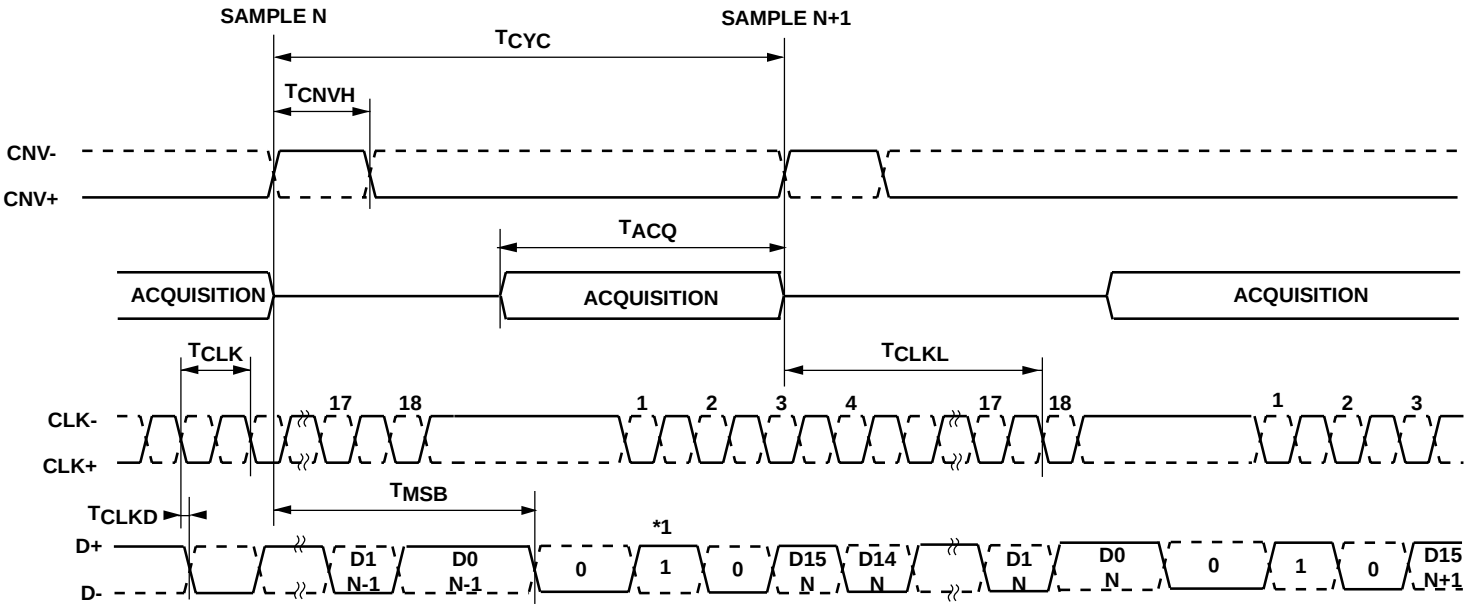
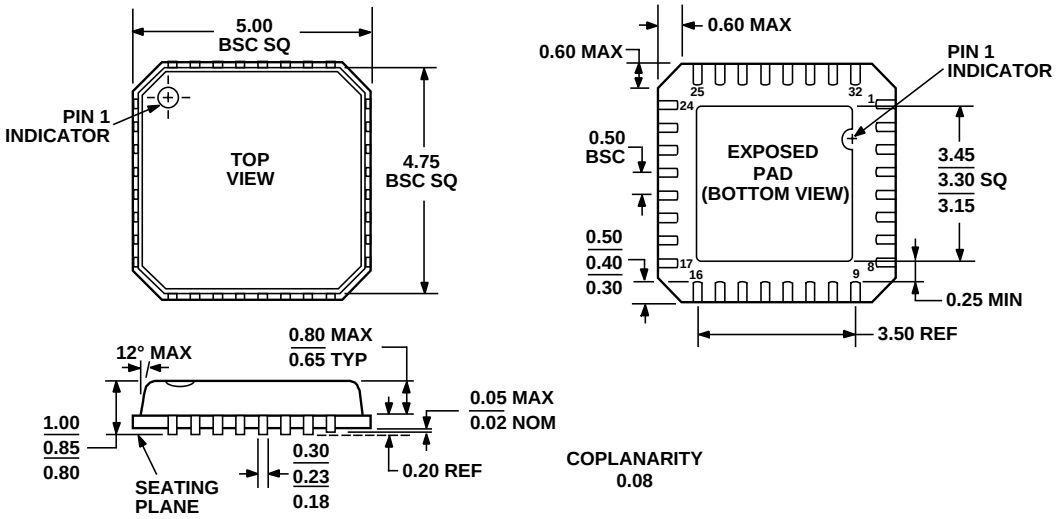


Figure 4. Self-Clocked Interface Mode Timing Diagram[1]

[1] This timing is for silicon rev 1 or above. For silicon rev 0, there is an extra bit (a zero) in front on the bit with value 1. Therefore, silicon rev 0 needs 19 clock pulses.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VHHD-2

Figure 5.32-Lead Lead Frame Chip Scale package [LFCSP_VQ]
5 mm × 5 mm Body, Very Thin Quad
(CP-32-3)

PR07652-0-6/08(PrB)